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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,038	06/27/2003	Chien-Chung Tseng	MXIC-P910232	8465

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,038	TSENG ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Nov 9, 2005 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-22,24-26 and 28-31* is/are rejected.

7)☒ Claim(s) *10,23,27 and 32-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/RCE

The amendment submitted on Oct 18, 2005, and the RCE submitted on Nov 9, 2005, have been reviewed and considered with the following results:

The RCE was approved and entered. Therefore, the amendment was also entered for further consideration.

The amended claims overcame the objections to claims 6 and 9, as described in the previous Office Action. Although those objections have now been withdrawn, various other objections were identified when all the active claims were carefully considered. These objections are described later under the appropriate section.

The amended claims also overcame all the rejections of the claims (2, 4, 13, 15, 17, 21, and 25) under 35 U.S.C. 112 as described on pages 3-4 of the previous Office Action. Those rejections have also been withdrawn. However, new rejections under 35 U.S.C. 112 are described later after all the active claims had been carefully considered.

Amended claim 1 overcame the rejections of claims 1-2, 4-5, and 7-8 under 35 U.S.C. 102(b), and the rejection of claim 3 under 35 U.S.C. 102(b)/103(a), all with respect to Smith et al. Therefore, those prior art rejections have been withdrawn since Smith does not clearly show or disclose the relationships between the first/second voltages with respect to the power-down/sleep modes as now recited within claim 1, upon which claims 2-5, and 7-8 depend.

Amended claim 10 overcame the rejection of claim 10 under 35 U.S.C. 102(b) with respect to the separate references of Savignac et al. and Giovinazzi et al. Those rejections have been withdrawn because neither reference clearly shows or discloses the relationships between

the reset signal, reference/first/second potentials, and the power-up/power-down states as now recited within the claim.

Amended claim 1 also overcame the rejection of claims 1-5, 7-8, and 14-19 under 35 U.S.C. 103(a) with respect to Slamowitz et al./Smith et al. Those rejections have now been withdrawn. Neither of these references clearly shows or discloses the relationships between the first/second voltages, and the power-down/sleep modes now recited within claim 1, upon which claims 2-5, 7-8, and 14-19 depend.

After reconsidering all of the active claims, some new prior art rejections have been made. These are described later under the appropriate section.

Claim Objections

Claims 1-10, and 12-34 are objected to because of the following informalities: To improve word flow, it is suggested a comma be added after "MOS devices" on line 2 of each of claims 1 and 26, and also after "V_t" on line 3 of each claim. Claim 1, line 7 should have --circuit-- added after "trigger" to ensure consistent labeling throughout the claims. Since claim 1 now recites "a sleep mode" on line 8, it is suggested "a sleep" in claims 7 (line 6), 9 (line 2), 19 (line 6), and 20 (line 4) be changed to --the sleep--. Claim 8, line 3 "a power-down" should be changed to --the power-down-- to clearly refer to the "power-down mode" now recited within claim 1. Claim 10, line 8 should have "a sleep" changed to --the sleep-- to clearly refer back to line 5's "a sleep mode." It is suggested --primary-- be added prior to "current path" on line 4 of claim 13 to clearly refer back to the only current path that has been identified (e.g. see line 2 of the same claim, and line 5 of claim 12). It is suggested "an" on line 4 of claim 20 be changed to

--the-- to more clearly relate "entering or exiting" back to the "enters and exits a sleep mode" phrase within claim 1, line 8. To improve word flow within claim 21, it is suggested --is-- be added prior to "operative" on line 2. Claim 23, line 8 "a sleep" should be --the sleep-- to clearly refer back to "a sleep mode" on line 5. It is suggested --primary-- be added prior to "current path" on line 4 of claim 25 to clearly refer back to the only current path that has been identified (e.g. see line 2 of the same claim, and line 5 of claim 24). Claim 31, line 4 should have --circuit-- added after "trigger" to ensure consistent labeling throughout the claims. The extra period at the end of claim 33 should be deleted.

Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9, 12-22, 24-25, and 28-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear how the threshold-enhancement node is structurally related to the Schmitt trigger circuit, and/or the voltage divider, within the power-on reset circuit recited within claim 1. For example, is the node part of the Schmitt trigger circuit, or is it separate from that circuit? It is not understood how "a first voltage" on line 3 of claim 7 relates to "a first voltage" now recited on line 6 of claim 1. For example, do they refer to the same voltage, or to different voltages? It is not clear how "a current" on line 5, and the two occurrences of "the current" on line 8, of claim 12 actually relate to one another, and to the

"primary current" of claim 10, line 3. For example, does each occurrence of "current" within claim 12 refer to the actual "primary current", only to a portion of it, or to a different current? Similar to claim 12 described above, how does "the current" on each of lines 2 and 3 of claim 13 relate to claim 10's "primary current"? It is not understood how "a first voltage" in claims 19 (lines 2-3), 20 (lines 2-3), and 22 (line 3) relates to "a first voltage" now recited on line 6 of claim 1. For example, do they refer to the same voltage, or to different voltages? It is not clear how "a second voltage" on line 4 of each of claims 21 and 22 relates to "a second voltage" now recited on line 7 of claim 1. For example, are they referring to the same voltage, or to different voltages? Also in claims 21 and 22, how does "a change of the supply signal" on lines 3 and 4-5 actually relate to one another? If the changes are not the same (e.g. one is an increase and one is a decrease), it is suggested "a change" on line 4 of each of claims 21 and 22 be changed to either --another change--, or to --a different change--. It is not clear how "a current" on line 5, and the two occurrences of "the current" on line 8, of claim 24 actually relate to one another, and to the "primary current" of claim 23, line 3. For example, does each occurrence of "current" within claim 24 refer to the actual "primary current", only to a portion of it, or even a different current? Similar to claim 24 described above, how does "the current" on each of lines 2 and 3 of claim 25 relate to claim 23's "primary current"? Since the voltage divider of claim 26 already comprises resistors, it is not understood how: 1) the "current source transistor" of claim 28, 2) the "low-side resistor" of claim 29, or 3) "compensate circuit" of claim 30, relates to them. For example, are these limitations additional elements within the voltage divider, or are they included with, or part of, the resistors?

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 6, 14, 17, 26, 29, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai, in view of Chou. Fig. 11 of Kawai shows a power-on reset circuit (e.g. see column 9, lines 46-56) comprising Schmitt trigger circuit 73 with its input coupled directly to resistors R1,R2 of voltage divider 70-72. However, Kawai does not show details of Schmitt trigger circuit 73, or clearly discloses power-down/sleep modes. Chou's reference shows and discloses various embodiments of a Schmitt-trigger circuit comprising a plurality of MOS transistors, all having the same threshold voltages (e.g. see column 3, lines 53-54, and column 4, lines 26-27). It would have been obvious to one of ordinary skill in the art to replace Kawai's (generic type) Schmitt trigger circuit 73 with one of Chou's specific Schmitt trigger circuits. Since voltage divider 70-72 will track supply signal +Vdd, and the Schmitt trigger circuit will

have a power reset trigger level (e.g. the point when the voltage applied to the input of the Schmitt trigger circuit will cause its output voltage to switch), claim 26 is rendered obvious. Chou's Schmitt trigger circuits are known circuits, and one of them can be used in Kawai's circuit as a means to consume less power, a desirable characteristic where power consumption can be critical. Resistor R2 of voltage divider 70-72 can be considered a low-side resistor for reducing leakage current (e.g. from capacitor 72), thus rendering claim 29 obvious. It is notoriously well known that a power-on reset circuit can have a power-down mode (e.g. when a power supply can be completely removed, or disconnected, from the circuit), and a sleep mode (e.g. when a power supply is reduced, wherein normal operation will still occur in most circuitry, but the lower power supply will inherently cause less power to be consumed). Therefore, it would have been obvious to one of ordinary skill in the art to apply that knowledge to the Kawai/Chou power-on reset circuit. During normal operation, +Vdd (corresponding to Chou's Vcc applied to the Schmitt trigger circuit) will be applied to the power-on circuit, thus allowing the threshold-enhancement node (between resistors R1-R2) to have a first voltage corresponding to the voltage drop within voltage divider 70-72. When the power-down mode is initially entered, +Vdd will still be at its normal voltage level, and the voltage at the threshold-enhancement node will be at its corresponding first voltage. After a period of time, first voltage will drop to ground due to the leakage current from capacitor C through resistor R2, since +Vdd will have actually been removed/disconnected completely from the circuit. When the power-down mode is exited, +Vdd will be returned to its normal voltage, allowing the threshold-enhancement node to return to its corresponding first voltage. Therefore, during the entering/exiting of the power-down mode, the threshold-enhancement node will effectively have

the first voltage, at least temporarily. When the sleep mode is entered/exited, +Vdd will be reduced, thus allowing the threshold-enhancement node to have a correspondingly lower voltage level, which can be deemed a second voltage. Therefore, claim 1 is rendered obvious. The use of power-down/sleep modes will provide a means for the power-on circuit to still perform its functions, while reducing the overall power consumption within the circuit. Voltage divider 70-72 comprises low-side resistor R2 for reduction of leakage current (for example, when initially powered down, R2 will effectively limit the amount of current leaking from capacitor C), rendering claim 4 obvious. When the threshold-enhancement node is at the first level corresponding to the normal +Vdd level, the first level will be greater than zero, and the second voltage (corresponding to when +Vdd is decreased in the sleep mode) will be less than the first voltage, rendering claim 6 obvious. It is notoriously well known that computer systems utilize power-on reset circuits to help ensure the system will not be placed into operation until the power supply voltage has reached a predetermined minimum level, which will ensure the system has sufficient power to operate properly. Therefore, it would have been obvious to use the Kawai/Chou power-on reset circuit in a computer system comprising a microprocessor, bus, and memory, thus rendering claim 14 obvious. This is considered intended use, as the power-on reset circuit will minimize the chance any erroneous switching, or operations, will occur within the computer system/microprocessor until the predetermined power supply level has been reached. Low-side resistor R2 renders claim 17 obvious for the same reason as described above with respect to claim 4. Claim 31 is rejected for the same reasoning as described above with respect to claim 6 (and its associated independent claim 1).

No claim is allowable as presently written, and claim 11 has been cancelled.

Allowable Subject Matter

However, claims 10 and 23 are only objected to, and would be allowed if their corresponding objection is satisfactorily addressed. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the method for providing a reset signal also includes the specific relationships between the reset signal, reference/first/second potentials, and the power-up/power-down states as recited within each of independent method claims 10 and 23.

Claims 27, and 32-34 are objected to as being dependent upon a rejected base claim, and for carrying over an objection from independent claim 26, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-3, 5, 7-9, 12-13, 15-16, 18-22, 24-25, 28, and 30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art references to ensure the power-on reset circuit, or the method for providing a reset signal, also includes: 1) the compensate circuit as recited within claims 2, 5, 15, 18, and 30; 2) the current source transistor as recited within claims 3, 16, and 28; 3) the reset signal node within the Schmitt trigger circuit as recited within claims 7-9, and 19-22; and 3) the primary current path and the compensating/compensation as recited within claims 12-13, and 24-25.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

20 January 2006

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Replacement Sheets

Figs 1-8B approved
1.20.06
TLE

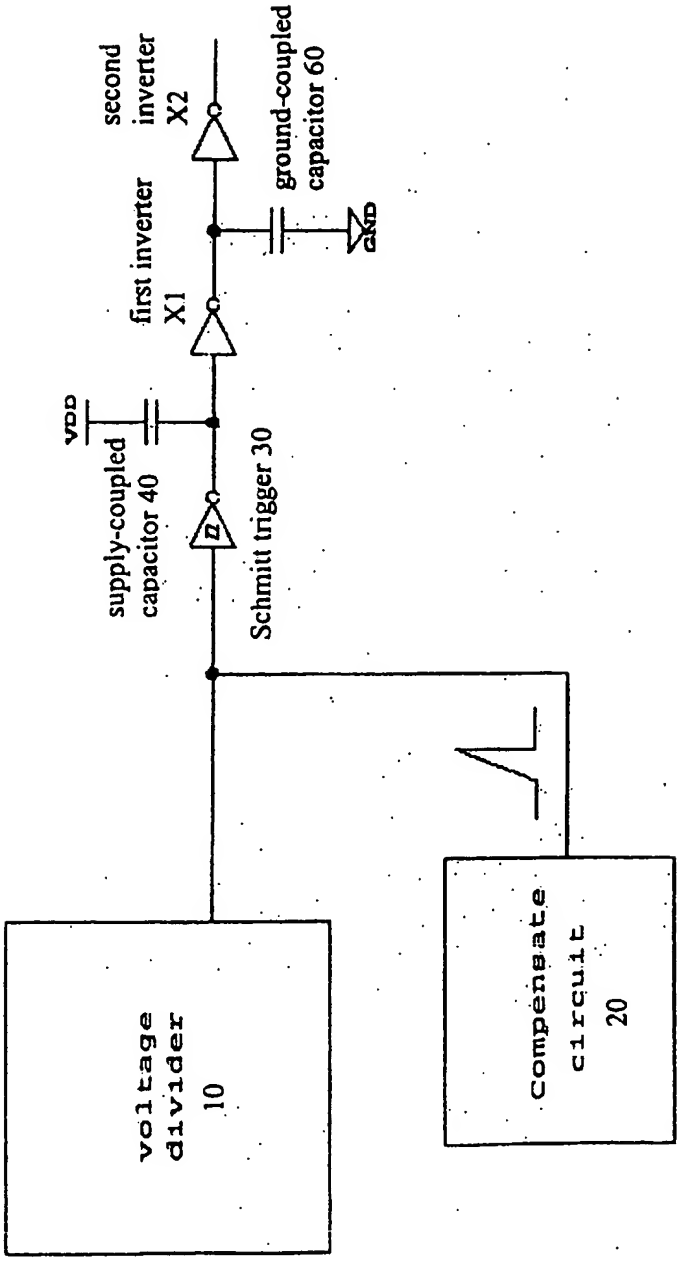

FIG. 1